

**ABSTRACT**

In particular, a system and method for receiving high speed processor bus  
5 traces for study of computer system capacity and operation uses a small FIFO  
memory and skips unused bus cycles to avoid the requirement for memory  
speed to match the processor bus speed. A time stamp is obtained to match  
each processor word to a time of occurrence to facilitate study of the trace data.  
Triggers are established to capture only those processor words that appear on  
10 the bus and which are also of interest. The remaining words are compacted by  
removing parts of the words that are not of interest from those words that remain  
in the queue based on the trigger criteria.